REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

Disposition of Claims

Claims 1-12 are pending in this application. Claims 1, 5, and 9 are independent. The remaining claims depend, directly or indirectly, from claims 1, 5, and 9.

Drawings

Applicant respectfully requests that the Examiner acknowledge whether the formal drawings filed on July 1, 2001 are acceptable.

Rejection(s) under 35 U.S.C § 102

Claims 1, 5, and 9 stand rejected under 35 U.S.C. § 102 (b) as anticipated by "Solaris Resource Manager – Controlling System Resources Effectively" (hereinafter "White Paper"). Claims 1, 5, and 9 have been amended to include the limitation "wherein allocating system resource comprises using a fair-share scheduler." Support for these amendments may be found, for example, in paragraph [0022] of the instant specification. No new matter has been added by the above amendments. To the extent that this rejection applies to the amended claims, the rejection is respectfully traversed.

In response to the Examiner's "Response to Arguments" section on pages 4-6 of the aforementioned office action, the Applicant respectfully maintains that the Examiner has incorrectly equated process groups with groups of users and that the Examiner has incorrectly asserted that White Paper teaches allocating system resources using the shares of the processor

sets allocated to the process group for the reasons previously discussed in the Response to Office Action mailed on May 7, 2004.

Further, the Applicant respectfully asserts that the Examiner's reliance on *In re Casey* is improper. Specifically, the Applicant respectfully notes that *In re Casey* is only applicable to rejections under 35 U.S.C. §103 and not 35 U.S.C. §102. Specifically, *In re Casey* addresses the applicability of 35 U.S.C. §103 rejections in circumstances in which the prior art references cited by the Examiner teach all the limitations of the claimed invention, but the invention is being used for a different purpose. In the instant case, the Examiner has rejected claims 1, 5, and 9 under 35 U.S.C. §102, thus, the reasoning of *In re Casey*, upon which the Examiner relies, is not applicable to the instant application.

The Applicant respectfully asserts that the appropriate legal standard for maintaining a rejection under 35 U.S.C. §102 is that White Paper must teach every aspect of the claimed invention either explicitly or impliedly, and any feature not directly taught must be inherently present.

The Applicant respectfully asserts that White Paper does not teach every aspect of the claimed invention as recited in the claims for at least the reasons previously discussed in the Response to Office Action mailed May 7, 2004. Moreover, even assuming *arguendo* that "process groups" and "groups of users" are equivalent, White Paper fails to teach or suggest "assigning each of said process groups a number of shares of at least one processor set." Rather, White Paper merely teaches assigning shares to "groups of users" (*see* White Paper, Figure 2-1 and the accompany text) with no mention of the processor sets.

Further, in response to the Examiner's contention that White Paper teaches allocating CPU resources to process groups by shares using Solaris Resource Manager which complements a number of products such as processor sets that SUN offers (Office Action, p. 5), the Applicant

respectfully asserts that mere mention of processor sets without any mention of allocating shares of processor sets to process groups does not satisfy the above legal standard for maintaining a rejection under 35 U.S.C. §102. The legal standard requires more than a mere reference to the name of an element. In particular, a mere reference to processor sets without any teaching or suggestion of allocating shares on the basis of processor sets and process groups does not amount to teaching each and every aspect of the invention as recited in the claims. In view of the above, White Paper does not support the rejection. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-12 stand rejected under 35 U.S.C. § 102 (e) as anticipated by U.S. Patent No. 6,714,960 ("Bitar"). Claims 1, 5, and 9 have been amended to include the limitation "wherein allocating system resource comprises using a fair-share scheduler." Support for these amendments may be found, for example, in paragraph [0022] of the instant specification. No new matter has been added by the above amendments. To the extent that this rejection applies to the amended claims, the rejection is respectfully traversed.

In response to the Examiner's "Response to Arguments" section on pages 4-6 of the aforementioned office action, the Applicant respectfully maintains that the Examiner's characterization of the teachings in Bitar is incorrect for at least the reasons previously discussed in the Response to Office Action mailed May 7, 2004.

In response to the Examiner's assertion in the "Response to Arguments" section in the Office Action mailed December 23, 2004, that the Applicant has merely alleged that the claims define a patentable invention, the Applicant has detailed the specific claim limitations that are not taught by Bitar. Bitar fails to teach or suggest at least the following claim limitations in independent claims 1, 5, and 9:

i) Bitar fails to teach "assigning each of said plurality of process groups a

number of shares of at least one processor set" (*see* Instant Application, claim 1). Specifically, Bitar fails to teach "process groups" and assigning shares for each of the multiple processor sets to each process group. Rather, Bitar teaches assigning shares to individual users (*see* Bitar, col. 4, ll. 54-60). Further, Bitar only teach associating a single job with shares from a single VMP (*see* Bitar, Fig. 1). In contrast, the above claim language clearly allows shares of multiple processor sets to be assigned to a single process group.

ii) Bitar fails to teach "wherein the allocating system resources comprises using fair-share scheduling." Specifically, Bitar does not teach or suggest fair-share scheduling, rather, Bitar only teaches "time-share scheduling" (*see* Bitar, col. 4, ll. 54-60). More specifically, fair-share scheduling enables a system to control the allocation of available CPU resources among processes (or process groups), based on their importance. This importance is expressed by the number of shares of CPU resources that are assigned to each process (or process group). In contrast, time-share scheduling allocates CPU time to teach process and then the processes are executed in order of the amount of time allocated to the process. Thus, processes allocated only small amounts of time are executed last. (*See* Bitar, col. 4, ll. 48-60).

In view of the above, Bitar does not support the rejection. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.554001).

Respectfully submitted,

Date: February 23, 2005

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